3x.9 High-Voltage Probe with High Input Impedance

Problem: Measure voltages or waveforms in a high-voltage circuit where the loading from even a 10 MΩ or 100 MΩ probe would be unacceptable. Solution: Come up with a circuit that can handle high voltages (and produce a $V_{in}/100$ "monitor" output), and which has input currents well below a microamp (and ideally down in the picoamp range). Happily, high-voltage MOSFETs provide a good solution. Here we'll evolve two approaches to the problem.

3x.9.1 Compensated-offset MOSFET follower

Figure 3x.76A shows a first stab, just a high-voltage MOSFET follower with 100:1 divider in the source terminal. It will work – sort of. But it has some serious problems: most obviously, the output drops to zero for inputs below some effective gate threshold voltage V_{th}; that is, there is no compensation for the non-zero error caused by V_{GS} offset. Furthermore, it suffers from a variable offset voltage (i.e., the MOSFET's changing V_{GS}) as the drain current goes from its maximum (here 100 μA at $V_{in} = 1$ kV) down to a microamp or less when the input is down around 10 V or less.

The basic source-follower idea can be improved considerably with the circuit modifications of Figure 3x.76B. A brief run-through of its operation goes like this: (a) We replace the source load of follower Q_1 with a current sink that returns to a low-voltage negative rail (to permit inputs down to zero), with the current set by low-voltage components A_3 and Q_3, assisted by high-voltage cascode MOSFET Q_2; next (b) we add to Q_3's emitter a correction current (via Q_4) that tracks the current diverted by the 100:1 output divider, so that follower Q_1 operates at a constant drain current (nominally 50 μA); next (c) we offset the bottom of the 100:1 divider with follower A_2 and Q_4 to cancel the (approximately constant) V_{GS} of Q_1; and finally (d) we calibrate the gain by trimming the divider ratio with R_6.

A few fine points: R_1 limits fault currents through protection diodes D_1–D_3; gate resistors R_2 and R_{13} suppress oscillation tendencies in the high-voltage MOSFETs; D_3 lowers the effective capacitance of zener D_2; and A_1's 50 Ω output resistor suppresses oscillation from external cable capacitive loading. See also §3x.6.5 for the use of series MOSFET stacks to go to higher voltages, and the use of higher currents for faster negative-slewing speeds.

3x.9.2 Bootstrapped op-amp follower

Here's an unusual circuit design (Fig. 3x.77) that puts an op-amp follower at center stage, assisted by high-voltage MOSFETs to bootstrap its supply rails to follow the input voltage. You can think of this as an op-amp-centric design, as contrasted with the MOSFET-centric design of Figure 3x.76. It's pretty daring – a low-bias 5 V CMOS op-amp handling input signals (and even abrupt steps) over nearly a kilovolt range. Scary enough in fact that we built and abused it mightily, and it just kept working.

The idea here is to leverage the accuracy and very low input current of a precision CMOS op-amp to achieve performance superior to that of the MOSFET follower. That's not hard to imagine – the LMP7721, for example, has a maximum input offset voltage of 0.15 mV, and a maximum bias current (at room temperature) of 20 *femto*amps (it claims *typical* values of 26 μV and 3 fA, damn impressive!).

So the basic circuit is just unity-gain follower U_1, with both full-swing and 100:1 outputs. Very clean, no offset trims, etc. The hard part is ensuring that the op-amp stays in its operating range and is not damaged by the worst possible insults at the input terminal. The op-amp's positive supply rail is created by depletion-mode follower Q_1, bootstrapped from the op-amp's output; that puts the rail typically 1–2 V above the op-amp output (it's a rail-to-rail op-amp, so there's no worry about headroom). Zener Z_1 sets the op-amp's total supply voltage, biased by depletion-mode current sink Q_2. The latter's current, nominally 1.5 mA, sets Q_1's operating current, and must be somewhat greater than the op-amp's quiescent current.[70]

You can kill a high-voltage circuit in an eyeblink, so we took pains to anticipate the worst: Diode clamps D_1 and D_2, with input current limited to less than a milliamp by the 1 MΩ input resistor, bound U_1's input voltage to no more than a half volt beyond the supply rails (and with any input current through U_1's input protection diodes kept below 0.1 mA by series resistor R_2). We've used the gate-channel diode of a small-geometry JFET for these clamp diodes, to minimize their contribution to the input current; at room temperature we measured leakage currents of just ∼ 20 fA with an applied voltage less than 3 V (see Figure 1x.120).

[70] We'd like to run at lower currents to minimize power dissipation in the MOSFETs, but we found that the low bandwidth of a micropower op-amp like the AD8603 ($I_Q \approx 40$ μA) caused oscillation in this circuit arrangement.

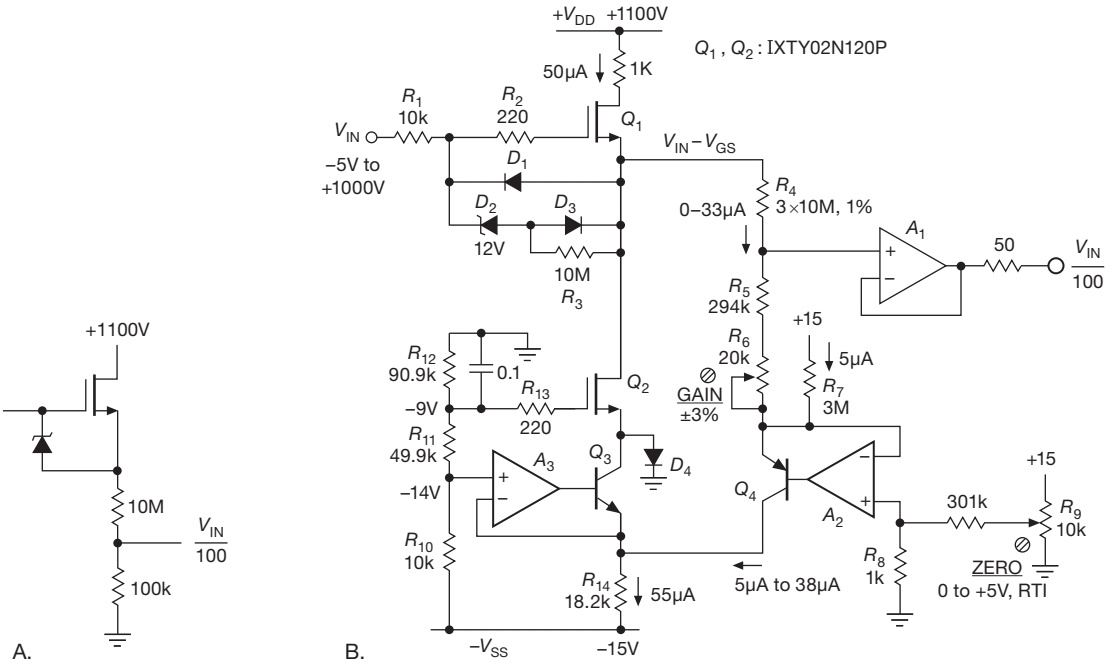

Figure 3x.76. High-impedance probes for input voltages to +1 kV. A. Simplest MOSFET follower. B. Cascode current sink biases MOSFET follower Q_1, with trim to cancel the V_{GS} offset of the latter.

Zeners Z_2 and Z_3 protect the MOSFET gates; note the polarity, appropriate for the depletion-mode's negative V_{GS}.

Finally, we added a 1 GΩ input bias path through R_7, so that an open input produces an output near ground. It can be returned to ground, if 1 GΩ is an acceptably high input resistance. Alternatively, R_7 can be bootstrapped as shown to produce an input resistance 1000 times higher (i.e., 1 TΩ). In the latter case the float voltage (referred to the input) is

$$V_{\text{float}} = 10^3 V_{\text{os}} + 10^9 I_{\text{bias}} \tag{3x.17}$$

(replace the factor 10^3 by unity if R_7 is returned to ground). For the component values here, and with an LMP7721 op-amp for U_1, that amounts to a worst-case float voltage (referred to the input) of ±150 mV (with bootstrapped R_7), or ±200 μV (with R_7 returned to ground).

In either case the probe's input current is

$$I_{\text{in}} = I_{\text{bias}} + \frac{V_{\text{os}}}{10^9} \tag{3x.18}$$

which amounts to a worst-case input current of ±200 fA.

Torture tests. This circuit worked nicely, doing what it was supposed to do. With a step input, measured rise and fall times were around 15 μs with the input resistor R_1 set at a conservative 1 MΩ; reducing R_1 to 100 kΩ speeded up the step response, to ∼2 μs for small steps (< ±100 V), but slew-rate limited for large steps (+100 V/μs and −50 V/μs).

We tried our best to destroy the prototype, by switching the input abruptly over a full swing (from zero to ±400 V); to ensure the fastest input slew rate we used a mercury relay, and banged the input repeatedly to a set of stiff positive and negative voltages. Figure 3x.78 shows some measured single-shot waveforms. These tests were a failure – we couldn't break the thing!

Extension to higher voltage. The voltage range of the circuit of Figure 3x.77 is limited by the voltage ratings of the depletion-mode MOSFETs, which for currently available parts top out at 1 kV.[71] You can extend the circuit to higher voltages, however, by spreading the voltage across several MOSFETs, a technique we've used earlier (e.g., see §3x.6.5 and Figures 3x.57 and 3x.61). And you can take advantage of the higher voltage ratings available in enhancement-mode MOSFETs – standard *n*-channel parts from IXYS go as high as 4500 V (see Table 3x.3).

Figure 3x.79 shows a simple extension of our probe circuit, to accommodate inputs to ±1 kV. Here Q_1 operates as before, bootstrapping the op-amp's positive rail; but di-

[71] We ran this circuit at somewhat lower voltage, because the measured drain curves rise rapidly as V_{DS} approaches 1 kV.

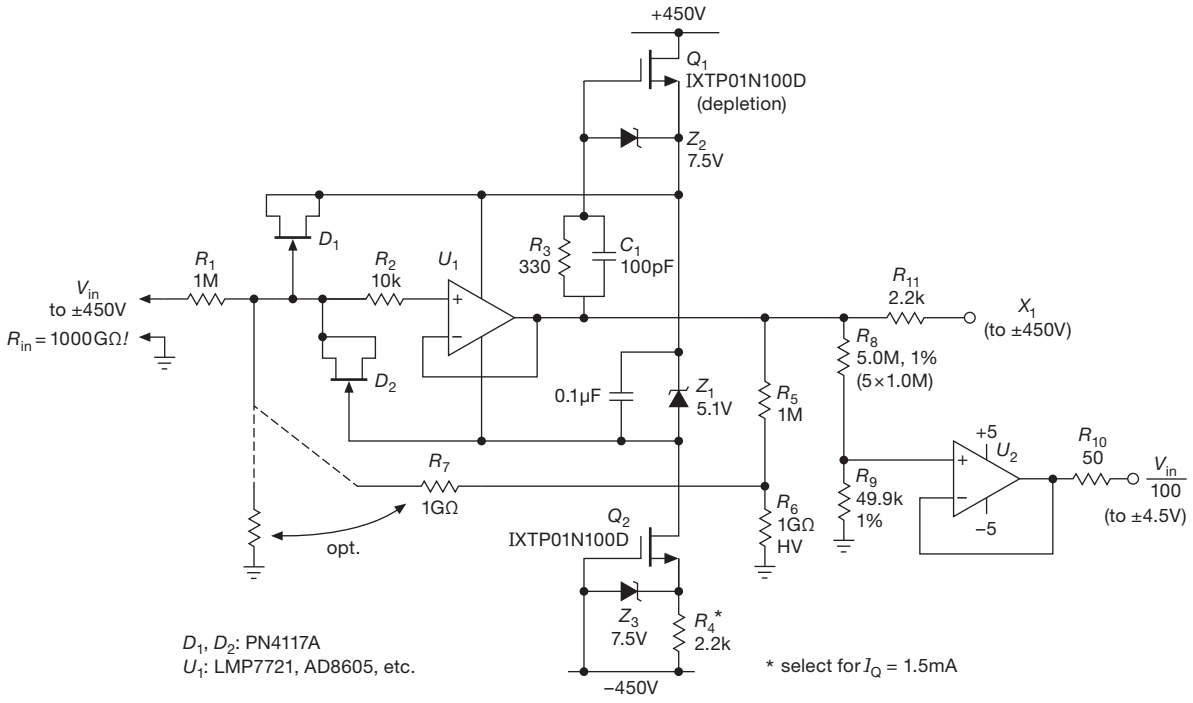

Figure 3x.77. Another high-voltage probe circuit, exploiting the accuracy of a low-I_b op-amp. The unusual bootstrap arrangement keeps the input signal within the op-amp follower's 5 V total supply.

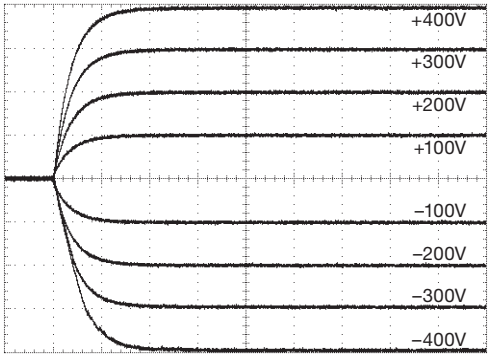

Figure 3x.78. Measured X1 output waveforms of the circuit of Figure 3x.77 when driven with abrupt steps to the voltages indicated. Vertical: 100 V/div; Horizontal: 20 μs/div.

vider $R_{12}R_{13}$ splits the span up to the positive HV rail, with enhancement-mode MOSFET Q_3 sharing the voltage burden. Down at the negative HV rail Q_2 is a current sink, with the voltage span assisted by Q_4. This time we've used a different scheme to set the sink current: instead of the not-very-predictable source self-bias arrangement (Q_2R_4 in Fig. 3x.77), we've used the LM334 programmable 2-terminal low-voltage current source (U_3) to set the sink current, with Q_2 acting as a cascode (a technique used earlier, in §3x.6.4). This scheme can be extended to higher voltages by stacking additional MOSFETs atop Q_3 and Q_4, or by substituting parts of higher voltage ratings, or both.

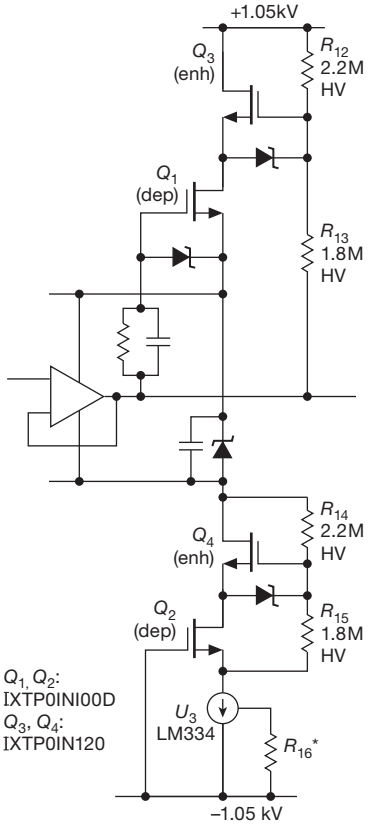

Figure 3x.79. Stacking a pair of cascode MOSFETs to Figure 3x.77 extends the voltage range to ± 1 kV.