4x.11 Rail-to-Rail Op-amps

We introduced RRIO op-amps in AoE's Chapter 4, and dealt with them in some detail in Chapter 5 (§5.9), where we discussed, among other things, their input and output properties. RRIO come not without some drawbacks, which we'll summarize here, for review, before exploring the very interesting topic of achieving "true" rail-to-rail output swing.

4x.11.1 Rail-to-rail inputs

Most rail-to-rail-input (RRI) op-amps use complementary pairs of differential input stages, which solves the problem of operation all the way to (and a bit beyond) each supply rail. But, as described in §5.9, this structure has some undesirable side effects, such as an abrupt change in input current (if BJT input transistors), an abrupt change in offset voltage, and a rise in distortion when input signals move through the crossover region. Figure 5.29 (duplicated here as Figure 4x.88) shows the disastrous degradation of offset voltage in two typical RRI op-amps, and a nice on-chip solution (internal charge-pump creation of a beyond-the-rail supply voltage, circumventing the need for paired complementary input stages).

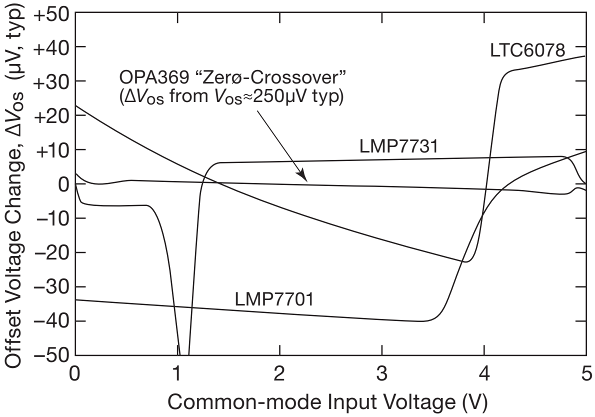

Figure 4x.88. Op-amps with rail-to-rail inputs usually exhibit a shift of $V_{\rm OS}$ as the input voltage passes control from one input pair to the other. The OPA369 circumvents this by using a single input pair, powered beyond the rail by an on-chip charge pump.

4x.11.2 Rail-to-rail outputs

Op-amps with rail-to-rail outputs suffer several drawbacks, mostly related to the common-source (or common-emitter) structure of the push–pull output stage, necessary to allow swings to the respective rails. The consequence is a high native output impedance (drain or collector), which means that the open-loop gain depends strongly on load impedance, and that a capacitive load creates undesirable phase shifts. The output stage also has inherently higher distortion, and, as we'll see next, in many cases it cannot swing *completely* to the rails (owing to quiescent current flowing through the output transistors' saturated $R_{\rm on}$).

4x.11.3 Output near ground: when "RRO" *isn't*

In §4x.3.8 we encountered a peculiarity (perhaps that's too diplomatic a term) of op-amps with rail-to-rail output stages, namely their inability to swing all the way to the negative supply voltage (i.e., ground, when powered from a single positive supply), even when the op-amp's output is unloaded. The deficit isn't large – typically a few millivolts – but it's enough to seriously compromise the dynamic range. Taking the example of the wide-range transimpedance amplifier in that discussion (Fig. 4x.35), where the op-amp's output is digitized by a modest 12-bit ADC with input span of 0 V to 4.095 V (thus an LSB of 1 mV), an op-amp that swings only to within 10 mV of ground is throwing away 3 bits (10 LSBs) of dynamic range. For a seriously accurate 16-bit ADC (a plausible choice since the LSB of 62 μV is comparable to worst-case offset errors in the suggested op-amp types), the inability of the op-amp outputs to go below 10 mV, say, corresponds to an ADC span of the bottom 160 LSBs.

It may seem puzzling that the output-stage nMOS pulldown switch (see Fig. 5.32B) does not go all the way to ground with no load attached. But it's not puzzling when you realize that output-stage quiescent current flowing through the on-resistance of the nMOS pulldown limits the negative swing to $V_{\rm min}{=}I_{\rm Q}R_{\rm ON}$. You can circumvent this problem with a current-sinking load, with current set to $I_{\rm Q}$ or greater.

We got interested in this problem, and rigged up some tests to explore the behavior of several interesting RRO op-amps. Figure 4x.89 shows what you get when you wire these as unity-gain followers, input grounded, and output connected to a current source varying from −0.5 mA (sinking) to +1 mA (sourcing). For example, our favorite jellybean LMC6482 sits at 7 mV (unloaded), going linearly to ground when 140 μA is sunk at its output. Evidently that's the quiescent current when the output is near ground. You can learn more: the slope of $V_{\rm out}$ versus $I_{\rm sink}$ reveals the nMOS output resistance, here about 57 Ω.

So, one way to make these puppies behave is to attach a current sink to the output; this requires a negative voltage source somewhere in the circuit.[64] If a negative voltage is not available, you can use a charge-pump voltage inverter to create it – see the short discussion in §4x.11.4, where we discuss also the (perhaps better) alternative of running the op-amp’s negative supply terminal a few tenths of a volt below ground.

Another possibility is to choose an RRO op-amp whose output is well behaved, as some in Figure 4x.89 appear to be. This eliminates the need for a negative supply, but it has the drawback of limiting your choice of op-amp types. We explored this scene for three of these RRO op-amps, wired as followers and driving each with a 25 mVpp triangle wave at 1 kHz. Figure 4x.90 shows the output waveforms under various load conditions (unloaded, resistor to ground, or current sink load), and with the input waveform just touching ground or with it offset so the negative peaks going 10 mV below ground.[65]

The top waveform is the input signal, when set for $V_{\rm min}{=}0$ V, used for all three parts shown in the lower panels. The LMC6482, whose curves in Figure 4x.89 predict failure near ground, bottoms out around 7 mV, even with a 1k load to ground (waveform A), but delivers clean waveforms to ground with a 200 μA sinking load (waveform B). In fact, it works well under this load (waveform C) even when the input triangle wave is offset to bring its negative peaks down to -10 mV.

Based on Figure 4x.89 we had hoped for better with the LTC6078; and its performance is pretty good (middle panel of Fig. 4x.90), but it flames out at around 1 mV (waveform A) unless a current-sinking load is attached (waveforms B and C). The AD8616, by contrast, heroically swings clear to zero on this scale (bottom panel, waveform A). Heroically, but not magically, as demonstrated by our attempt to have it do the impossible with a negative input (waveform B) but without a current-sinking load; but the clean saturation without evidence of recovery transients is admirable. As with the other op-amps, a current sink at the output (here requiring nearly a milliamp) allows it to swing negative.

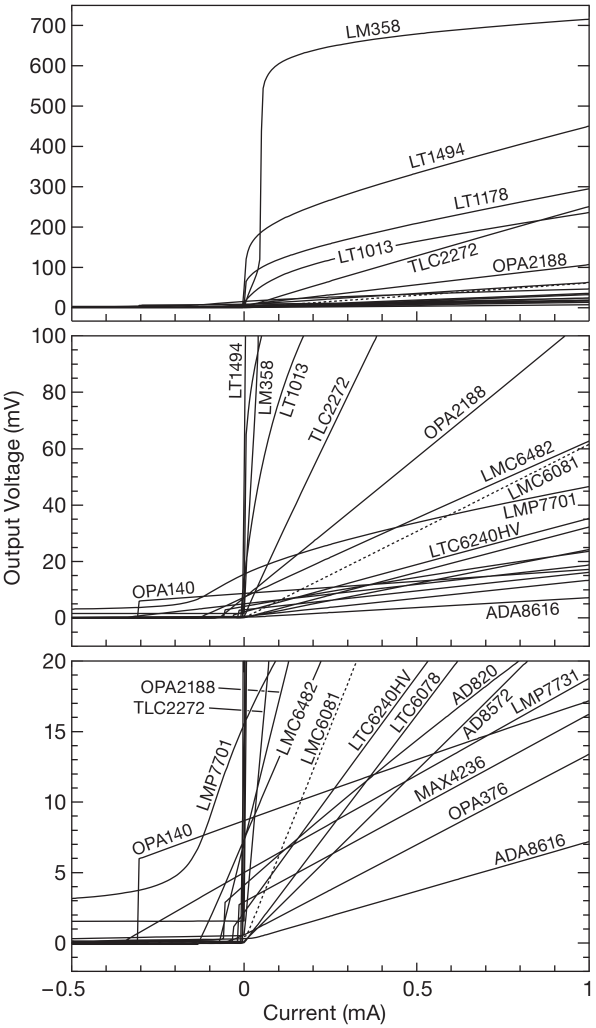

Figure 4x.89. Not all op-amps that specify output swing to the negative rail (including RRIO and RRO types) will reach that voltage, as seen in these plots of $V_{\rm out}$ versus $I_{\rm load}$ for 18 representative op-amp types. For these plots the op-amps were wired as followers with grounded input, with $V_+{=}5$ V and $V_-{=}0$ V.

Instead of a current sink at the op-amp’s output, you can simply supply a slight negative voltage (100 mV, say) to the op-amp’s negative supply terminal. This method works for any single-supply components (comparators, ADCs, etc.) that are struggling in those last few millivolts near ground; we discuss it next.

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[64] A simpler solution you might invent is a simple resistor to ground, but it does not work: even a small value like 1 kΩ sinks only 10 μA when the output is 10 mV above ground, far less than the quiescent current you’re trying to cancel.

[65] We were interested in the latter because we worried about the dynamic behavior of a feedback circuit where the input voltage may flirt with ground, causing the output to saturate at zero volts. Such a nonlinear situation allows for no overshoot, and could exhibit unwholesome behavior.

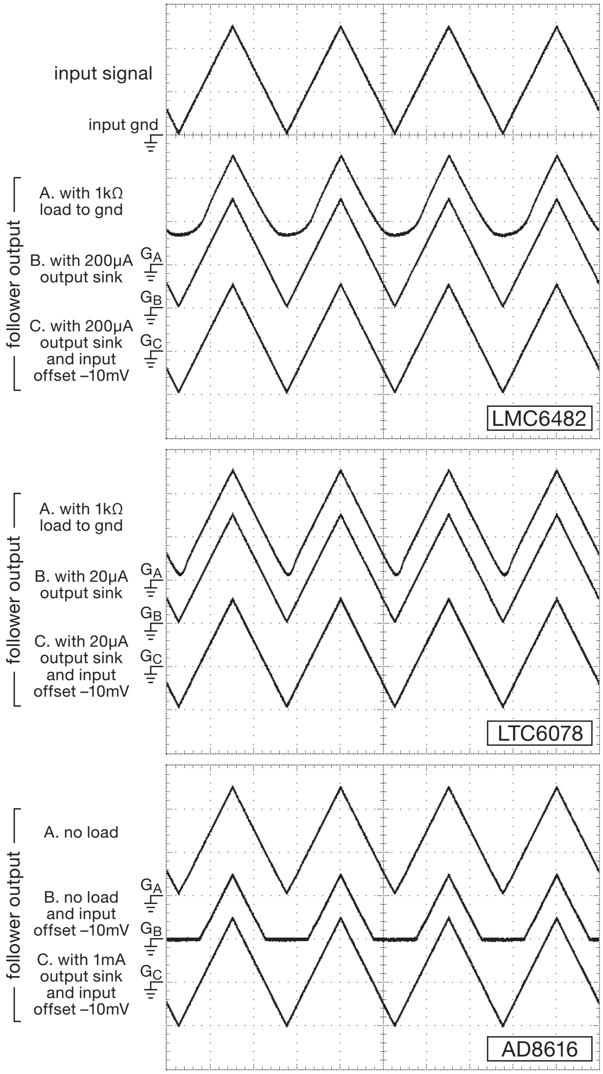

Figure 4x.90. Three RRIO op-amp followers, powered from +5 V and ground, and driven with a 25 mV triangle wave whose negative peaks are at ground or offset to −10 mV. The output waveforms correspond to open, resistive, or current-sinking loads, as indicated. Vertical: 10 mV/div; horizontal: 400 μs/div.

4x.11.4 Offsetting the negative supply terminal

In the good ol' days of ±15 V supply rails we never worried about behavior near ground; couldn't care less. But it's a real issue with single-supply designs, and particularly low-voltage parts; there RRO and RRIO op-amps will get you to ground … almost. As we discussed in the previous section, most RRO op-amps flame out a few millivolts above the negative (i.e., ground) rail. Not bad, but a serious drawback if you're needing the full dynamic range, as we did in the wide-range TIA circuits of §§4x.3.7 and 4x.3.8. As we saw, one solution is to sink some current from the output. A more general solution, which deals also with close-to-ground problems in other single-supply parts (like comparators and single-supply ADCs) is to supply a small negative voltage to the part's negative supply pin.

If you've got a negative voltage available, you can generate a $\sim$250 mV negative supply by simply biasing a Schottky diode into forward conduction: an SD103 diode, for example, has a forward drop of 250–300 mV at 5 mA (a 1N5817 drops 175–225 mV at 10 mA). We used this idea in Figure 4x.91B, where we show also a flying-capacitor voltage inverter to generate the necessary negative rail. That figure shows the very nice LTC1550 part,[66] which includes a linear post-regulator for low ripple and noise; its 900 kHz oscillator frequency lets you use pleasantly small-value (0.1 μF) flying capacitors.

Evidently the need for low-voltage negative supplies has not escaped the semiconductor industry, who offer the LM7705 voltage inverter illustrated in Figure 4x.91A. It also includes a linear post-regulator, but set to −230 mV. This part is small and inexpensive ($0.66 in unit quantities), but does require large-value capacitors because of its lower operating frequency (92 kHz). It was clearly designed for exactly this purpose; the datasheet says it all:

> The LM7705 device is a switched capacitor voltage inverter with a low noise, −0.23 V fixed negative voltage regulator. This device is designed to be used with low voltage amplifiers to enable the amplifier's output to swing to zero volts. The −0.23 V is used to supply the negative supply pin of an amplifier while maintaining less than 5.5 V across the amplifier. Rail-to-Rail output amplifiers cannot output zero volts when operating from a single-supply voltage and can result in error accumulation due to amplifier output saturation voltage being amplified by following gain stages. A small negative supply voltage… will help maintain an accurate zero through a signal processing chain. Additionally, when an amplifier is used to drive an input of the ADC, the amplifier can output a zero voltage signal and the full input range of an ADC can be used.

Note that the increment to the "total supply voltage" is so small that you don't have to decrease the positive supply voltage: you can still use a +5 V positive rail for a low-voltage part that specifies supply voltages from 2.7 V to 5.5 V, for example.

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[66] We show the −2.5 V part, but you can get other pre-set voltages, or an adjustable part with 1.22 V internal reference.

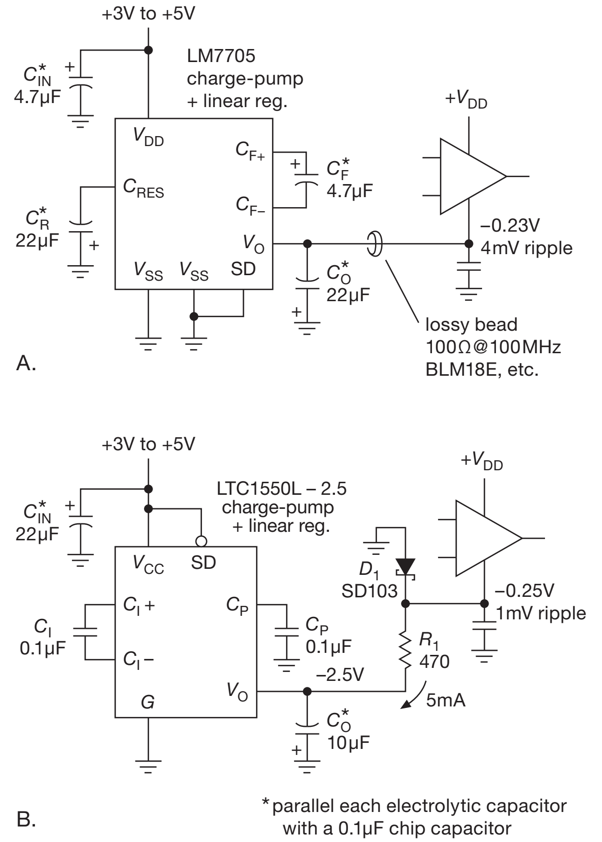

Figure 4x.91. Charge-pump voltage inverters are a nice way to generate a ~0.25 V negative rail, so RRO op-amps (and other parts) can operate cleanly to zero volts.

4x.11.5 Designs by the masters: the Monticelli output stage

The output stage of a conventional (not RRO) op-amp is ordinarily a complementary push–pull follower (or some variation thereupon), biased with some conduction overlap to prevent crossover distortion at mid-supply (see §5.8.3). By contrast, the output complementary pair in an RRO op-amp is configured as a push–pull common-source *amplifier*, see Figure 5.32. That's necessary for the output to reach the rails (absent a second set of beyond-the-rails supply voltages). But it creates problems, owing to its inherently high output impedance. Some of these (described in §5.8.3) are high open-loop output impedance, especially at low frequencies; instability with capacitive loads; and dependence of open-loop gain on load resistance.

The rail-to-rail output stage also presents challenges to the chip designer when it comes to quiescent biasing and reduction of crossover distortion. An elegant solution is the output stage designed by Dennis Monticelli, described briefly (in the context of low-distortion) in §5.9.2.[67] At the broad brush-stroke level, it is a clever circuit that biases the push–pull output transistors to maintain current overlap at crossover, and, better still, with continuing current through both transistors *throughout the output swing*. Read the basic description in §5.8.3 first, then join us for an exploration of its detailed workings.

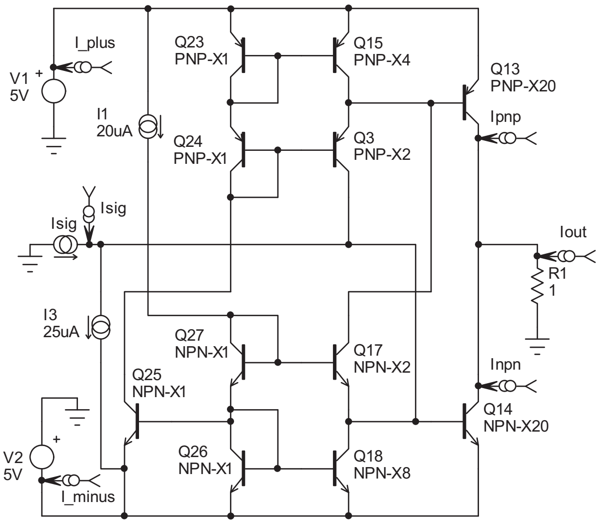

Figure 4x.92. SPICEing the Monticelli rail-to-rail output stage. Both input and output signals are *currents*, effortlessly probed by plopping down a "current probe" (if only real life were that simple!).

This is one cool circuit! We ran a SPICE simulation, to check out its linearity, and to see the overlap of source and sink currents over the full swing. Figure 4x.92 shows the circuit, as entered in IntuSoft's ICAP/4 SPICE software.

First we explored the transfer function, by sweeping the input current and watching the output current and the individual source and sink currents. In Figure 4x.93 the output current looks quite linear, to the eye. Also, you can see (maybe) that both transistors stay in conduction (just barely) over the full cycle. To explore this latter point, we plot in Figure 4x.94 the source ($I+$, from Q_{13}) and sink ($I-$, from Q_{14}) currents versus output current I_{out},

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[67] See his patent US4570128, and his IEEE *JSSC* paper (SC-21, #6, 1986), in which he says "The output stage (Figure 8) must solve a level shifting problem that has plagued rail-to-rail designs for some time. Elaborate solutions have been proposed that combine multiple embedded feedback loops that are in effect op amps within op amps. To succeed as a general-purpose quad, a simpler solution had to be found." Although originally developed at NSC, this circuit (or close variations) is popular with op-amp designers at Analog Devices and at TI (even before it swallowed NSC).

on both coarse and expanded scales; the latter shows the 100 μA–200 μA current in the "wrong" transistor. By comparison, these currents drop fully to zero in a normal class-AB push–pull output stage, as shown in the corresponding SPICE simulation of Figure 4x.95.

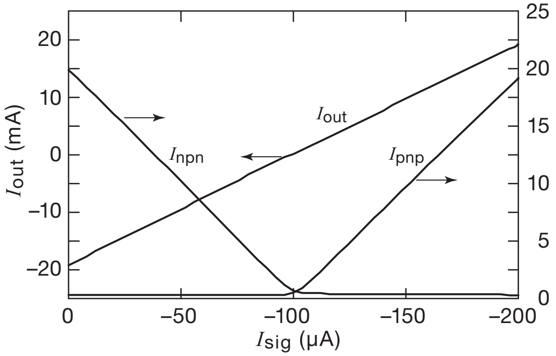

Figure 4x.93. Source, sink, and output currents for a BJT implementation of the Monticelli rail-to-rail output circuit, as modeled in SPICE.

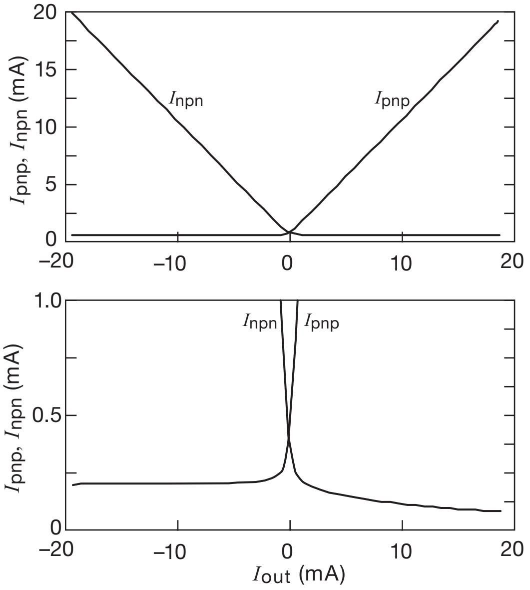

Figure 4x.94. Source and sink currents versus output current for the Monticelli circuit simulation. Note that both transistors remain in conduction over the full cycle.

Seeing this circuit being adopted by many designers of high-performance op-amps in the last 25 years, we continue to be impressed by Monticelli's creation. He originally developed the circuit to work with silicon-gate MOSFETs, but it works especially well with BJTs. His circuit is perfectly suited for balanced push–pull drive (to the bases of Q_{13} and Q_{14}, in Fig. 4x.92). It works well at high frequencies – for example, the OPA1611 has an 80 MHz GBW, and it can deliver lots of output drive (the OPA209 is happy delivering 65 mA, which is plenty for a 40 V op-amp).

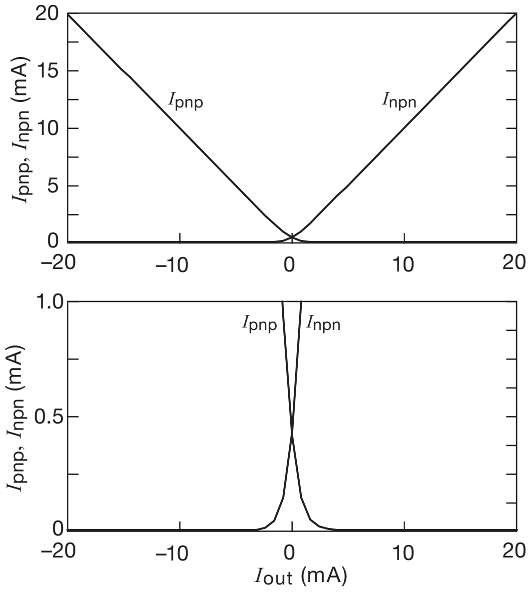

Figure 4x.95. By contrast, the currents in a conventional class-AB push–pull follower output stage go completely to zero beyond the narrow crossover region, as seen in the SPICE simulation of the circuit of Figure 5.32.

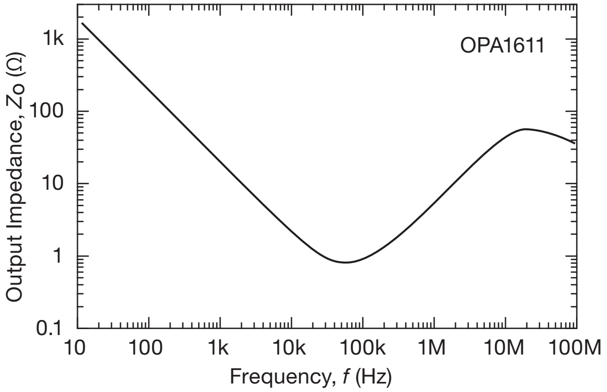

Figure 4x.96. Open-loop output impedance of the OPA1611 op-amp, which incorporates a Monticelli output stage (with capacitive feedback to lower the output impedance).

Many op-amp datasheets don't reveal the inner workings of their output stage, but sometimes you can recognize a

Monticelli rail-to-rail output stage from a distinctive open-loop output impedance versus frequency plot. Many of the TI op-amps with a Monticelli output stage add an output feedback capacitor to an input-stage gain node, which causes Z_{out} to drop to an amazingly low value, e.g., 1 Ω at 100 kHz for the OPA1611, before rising and then falling again; see for example Figure 5.34 in AoE3, or Figure 28 from the OPA1611 datasheet (plotted here as Fig. 4x.96).